IN THE CLAIMS:

In accordance with the Revised Rules under 37 C.F.R. 1.121, please amend the claims as shown below and indicated as "currently amended." Also shown below are claims that may be original, cancelled, withdrawn, previously presented, new, and not entered.

1. (currently amended) A digitally controlled oscillator for generating a correct-phase output signal at a desired frequency, having an input for supplying a digital input word, an adder for summing the digital input words, a stable local oscillator for supplying a clock signal at a constant frequency, and a delay circuit which comprises a coarse delay stage having a plurality of series-connected coarse delay elements and a fine delay stage having a plurality of series-connected fine delay elements, ~~where the coarse delay stage and the fine delay stage are designed~~ such that the total delay of the coarse delay stage and the fine delay stage is proportioned such that the maximum total delay and the minimum total delay of the delay circuit differ by no more than one period of the clock signal, and where the plurality of fine delay elements corresponds to the delay by one coarse delay element, wherein each coarse delay element includes a corresponding dedicated actuatable selector and each fine delay element ~~comprises~~ includes a corresponding ~~a~~ dedicated actuatable selector.

2. (previously presented) The digitally controlled oscillator as claimed in claim 1, in which the coarse delay element comprises a delay element and the selector, with one input on the selector in the respective coarse delay element being connected to the output of the delay element of the same coarse delay element and a further input on the selector being connected to the output of the selector in the coarse delay element connected immediately downstream.

3. (previously presented) The digitally controlled oscillator as claimed in claim 1, wherein

the fine delay element has a common input and at least two drivers connected to the common input, with a capacitive load being provided at the output of one of the two drivers, which oscillator also has one input on the selector connected to the output of the driver without the capacitive load and a further input on the selector connected to the output of the driver with a capacitive load, and which oscillator has the output of the selector in the respective fine delay element connected to the common input of the fine delay element connected immediately downstream.

4. (previously presented) The digitally controlled oscillator as claimed in claim 1, wherein the fine delay element comprises a plurality of drivers whose inputs are connected to one another to form a common input and whose outputs are connected to one another to form a common output, in which also the selector is designed such that the individual drivers may be activated or deactivated, and in which the common output is connected to the common input of the fine delay element connected immediately downstream.

5. (previously presented) A digital phase trimming circuit (PLL), having an input clock signal, having a phase comparator, a filter, a digitally controlled oscillator, and a feedback path which feeds back an output signal generated by the digitally controlled oscillator to the phase comparator, including frequency multiplication and/or frequency division, wherein the digitally controlled oscillator is designed in accordance with claim 1.